X-late (non-rush)



# SEMICONDUCTOR DEVICE AND ITS PRODUCTION


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Equivalents: JP2991753B2


## Abstract


PURPOSE:To reduce chip size by providing a second conductivity type extended drain area which contacts with a drain contact area, providing a first conductivity type area which is biased reversely to the extended drain area in the extended drain area and permitting the surface of a semiconductor substrate between the extended drain area and a source area to be a channel area so as to provide a gate electrode on the channel area through a gate oxide film.

CONSTITUTION:Boron is ion-implanted in an extended drain area 11, some heat processing is performed, then, the surface of a semiconductor substrate 15 is thermally oxidized. Thus, the segregation coefficients of the boron in a silicon oxide film 8 and the boron in silicon are differentiated. Thus, the boron density at the surface of the substrate 15 is reduced to be N-type and a P-type area is buried in the extended drain area 11. The P-type area 10 is biased reversely to the drain area 11 and depletion layers are spread between the extended drain area 11 and the semiconductor substrate 15 and between the P-type area 10 in the extended drain area 11 and the extended drain area 11. Therefore, the on-resistance between the drain sources becomes smaller than the MOSFET of the conventional structure.

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(54) Title of the Invention: SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

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Specifications

1. Title of the Invention: Semiconductor Device And Its Manufacturing Method

2. Scope of the Patent's Claims

(1) A semiconductor device, having a construction wherein an extended drain region of the second conductive type is created adjacent to a drain contact region between the drain contact region and a source region of the second conductive type, mounted on a semiconductor substrate of the first conductive type;

a first electrode having a reversed bias to the extended drain region is deployed in this extended drain region;

a semiconductor substrate is used as a channel region between the extended drain region and the source region;

and a gate region is deployed through a gate oxide film on this channel region

(2) A method to manufacture a semiconductor device as an N-type channel MOSFET described in claim 1,

wherein an extended drain region is formed when a P-type region is formed as the first conductive type region in the N-type extended drain region so that it is biased reversely to this drain region;

which is followed by implanting boron ions in order to form a P-type region;

and the density of the P-type region is reduced below that of the surface of the extended drain in order to confine the P-type region inside the extended drain region.

3. Detailed Explanation of the Invention

This invention relates to a semiconductor device, in particular a semiconductor device that can be used as a MOSFET when it is necessary to increase breakdown voltage between the drain and the source.

Prior Art Technology

Figure 2 shows a profile view of a high-resistance type of a MOSFET according to prior art. In order to increase the breakdown voltage between the drain 20 and the source 23, an extended drain region 21 having a low impurity content is formed in a semiconductor substrate 25, and reversed bias is applied between the drain 20 and the source 23 in order to widen the depletion layer on the extended drain region 21. In addition, as shown in the figure, 16 is a drain electrode, 17 is a source electrode, 18 is a silicon oxide film, 19 is a gate electrode, 22 is an anti punch-through region, and 24 is a substrate contact region.

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Problem To Be Solved By This Invention

Although a widening depletion layer was created through the junction between the extended drain region 21 and the semiconductor substrate 25 when an extended drain region construction was created as explained above, it was necessary to reduce the concentration in the extended drain region 21 so as to create the depletion design of the extended drain region 21 in order to increase the breakdown voltage between the drain 20 and the source 23. And although this made it possible to realize a high resistance, the resistance component was increased in the extended drain region 21, and the on-resistance was thus increased between the drain 20 and the source 23 of the MOSFET. This created a large loss during operations and a large size of the components was required to permit the flow of high currents.

Means To Solve Problems

In order to solve the above described problem, the present invention uses a construction wherein an extended drain region of the second conductive type is created adjacent to a drain contact region between the drain contact region and a source region of the second conductive type, mounted on a semiconductor substrate of the first conductive type;

a first electrode having a reversed bias to the extended drain region is deployed in this extended drain region;

a semiconductor substrate is used as a channel region between the extended drain region and the source region;

and a gate region is deployed through a gate oxide film on this channel region.

Operation

Because this invention has the above described construction, this not only makes it

possible to realize a high resistance, but also to greatly reduce the on-resistance between the drain and the source.

Embodiment

Figure 1 shows a profile view of an N-channel MOSFET of one embodiment of the semiconductor device of this invention. Using a surface density of the extended region 11 of approximately 1 x $10^{16}$ $cm^{-3}$, a P-type region 10 was formed in this extended drain region with a density of at least 5 x $10^{16}$ $cm^{-3}$. The density of the semiconductor substrate 15 was selected as 3 x $10^{14}$ $cm^{-3}$ and the thickness of a silicon oxide film 8 on the surface of the semiconductor substrate 15 was selected as at least 2 Φm. A polycrystalline silicon film was used for the gate electrode 7. The silicon oxide film located under the gate electrode created a gate oxide film. To form the P-type region 10, first, ions were implanted in the semiconductor substrate 15 of the extended region 11 and after an impurity dope region was formed by diffusion, boron ions were implanted in the extended drain region 11 for impurity doping of the P-type region 10 so that after a small amount of heat processing was conducted, heat oxidation of the surface of the semiconductor substrate 15 was performed. Because this created a different segregation coefficient of the silicon oxide film 8 and of silicon, the boron concentration was reduced in the surface of the substrate 15, creating an N-type construction, while the construction of the P-type region was created confined to the extended drain region 11. The P-type region 10 was provided with a reversed bias to that of the drain region 11, and a wide depletion layer was created between the extended drain region 11 and the semiconductor substrate 15, and between the P-type region 10 in said extended drain region 11 and the extended drain region 11. Accordingly, unlike with a construction according to prior art, the depletion layer design can thus be created in the extended drain region 11 even if a high density is used in the extended drain region 11. Therefore, this makes it possible to reduce the on-resistance between the drain and the source below the resistance of a MOSFET construction according to prior art. It thus become possible to reduce the resistance between the drain and the source per a unit of surface area to 1/5 ~ 1/6 when compared to a MOSFET construction according to prior art.

Effect of The Invention

As was explained above, the present invention makes it possible to shrink the size of a horizontal MOSFET chip of the high resistance type.

4. Brief Description of Figures

Figure 1 shows a profile view of the N-channel MOSFET type according to one embodiment of the present invention, Figure 2 shows a profile view of a high-resistance horizontal MOSFET according to prior art.

1 ... drain terminal, 2 ... P-type region electrode terminal in extended drain, ... 3 ... gate electrode, 4 ... source electrode, 5 ... drain electrode, 6 ... source electrode, 7 ... gate electrode, 8 ... silicon oxide film, 9 ... drain contact region, 10 ... P-type region in the extended drain region, 11 ... extended drain region, 12 ... anti punch-through region, 13 ... source region, 14 ... substrate contact region, 15 ... semiconductor substrate.

Representative's Name: Akira Kokeji, patent attorney, 2 others.

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Figure 1

| | | |
|---|---|---|
| 1 | ... | drain terminal |
| 3 | ... | gate terminal |
| 4 | ... | source terminal |
| 5 | ... | drain electrode |
| 6 | ... | source electrode |
| 7 | ... | gate electrode |
| 8 | ... | silicon oxide film |
| 9 | ... | drain contact region |
| 10 | ... | P-type region |
| 11 | ... | extended drain region |
| 12 | ... | anti punch-through region |
| 13 | ... | source region |
| 14 | ... | substrate contact region |
| 15 | ... | semiconductor substrate |
| 30 | ... | channel region |

Figure 2


| | |
|---|---|
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H01 29/78 301 X

PROCEDURAL AMENDMENT

[stamp] APPLICABLE

To: The Commissioner of the Japan Patent Office

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1. Item Description: Japanese Patent Application Number 2-225797

2. Amending Party:
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4. Number of claims added by the amendment: 4

5. Name of amended document: Specifications

6. Amended item: Scope of the Patent's Claims

7. Content of the amendment:

The content of the Scope of the Patent Claims in the Specifications is amended in the enclosed Appendix.

2. Scope of the Patent's Claims

(1) A semiconductor device, wherein a source of the second conductive type is formed on a substrate of the first conductive type, together with a an extended drain region of the second conductive type, a channel region is created between said source region and said extended drain region, and a drain contact region is created in said extended drain region;

wherein the first conductive region is created between said drain contact region and said channel region in said extended drain region.

(2) The semiconductor device described in claim 1, wherein the first conductive type region is created confined to said extended drain region inside the extended drain region.

(3) The semiconductor device described in claim 1, wherein the first conductive type region created inside the extended drain region is biased reversely to said extended drain region.

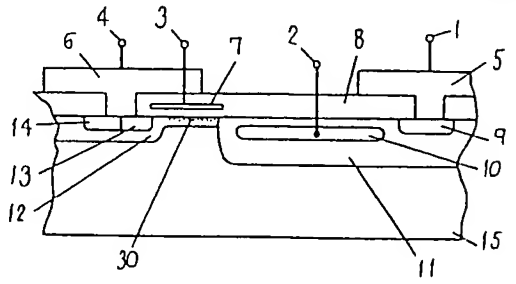
(4) The semiconductor device described in claim 2, wherein the first conductive type region created inside the extended drain region is implanted with boron ions.

(5) A method to manufacture the semiconductor device described in claim 1, comprising a step in which an extended drain region of the second conductive type is created, and a step in which the first conductive region in said extended drain region is implanted at least with boron ions.

(6) The method to manufacture the semiconductor device described in claim 5, wherein said first conductive type region is formed by oxidation of the ion-implanted surface of the second conductive type region after formation with ion implantation of the first conductive type region.

1…ドレイン端子
3…ゲート端子
4…ソース端子
5…ドレイン電極
6…ソース電極
7…ゲート電極
8…シリコン酸化膜
9…ドレインコンタクト領域
10…P型領域
11…延長ドレイン領域
12…アンチパンチスルー領域
13…ソース領域
14…基板コンタクト領域
15…半導体基板
30…チャネル領域

第 1 図




第 2 図